

Application Serial Number 10/535,566
Response to Office Action
Dated August 30, 2006

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1. Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A driver comprising:

a first current source[[]];

an output transistor, operably coupled to the first current source[[]];

a mirror transistor, wherein the first current source includes a first amplifier that is configured to: compare an output voltage of the output transistor to a reference voltage, and, provide a driving current to the output transistor when the output voltage of the output transistor is above the reference voltage[[]]; and

a switch that is configured to selectively couple the mirror transistor and the output transistor to form a first current mirror that controls bias current through the output transistor.

2. (Cancelled).

3. (Currently Amended) The driver of claim [[2]]1, wherein the driving current is substantially constant.

4. (Currently Amended) The driver of claim [[2]]1, further including a second current source that is configured to provide load current to a load that is coupled to the output transistor.

5. (Previously Presented) The driver of claim 4, wherein the second current source

Application Serial Number 10/535,556
Response to Office Action
Dated August 30, 2006

includes a second amplifier that is configured to provide the load current to the load when the output voltage is substantially equal to the reference voltage.

6. (Previously Presented) The driver of claim 5, further including a controller that is configured to maintain a minimal current to the output transistor that prevents the output transistor from turning off.

7. (Previously Presented) The driver of claim 4, wherein the second current source is further configured to provide the bias current to the output transistor.

8. (Previously Presented) The driver of claim 7, further including a compensation circuit that is configured to control the bias current substantially independent of process variations and temperature.

9. (Previously Presented) The driver of claim 4, wherein the second current source includes a blocking diode that isolates the driver from voltages applied to the output transistor from sources external to the driver.

10. (Previously Presented) The driver of claim 4, wherein the output transistor is of a first channel-type, and the second current source includes a transistor of a second channel-type that differs from the first channel-type.

11. (Currently Amended) The driver of claim [[2]]1, wherein the first amplifier is configured to provide configurable gain.

12. (Previously Presented) The driver of claim 1, wherein the first current source includes a second current mirror, that provides the bias current to an input of the first current mirror, and a third current mirror that provides the bias current to an output of the first current mirror.

Application Serial Number 10/535,556
Response to Office Action
Dated August 30, 2006

13. (Previously Presented) The driver of claim 1, wherein the mirror transistor and the output transistor are sized so that the bias current provides a gate-source voltage that is above a threshold voltage of the output transistor.

14. (Previously Presented) The driver of claim 1, wherein the output transistor is configured to have a Miller capacitor coupled between a drain of the output transistor and a gate of the output transistor.

15. (Currently Amended) A driver comprising:

a first current source;

an output transistor having a gate operably coupled to the first current source, a drain operably coupled to a first node of a bus, and a source operably coupled to a second node of a bus, wherein the first current source includes a first differential amplifier having: a first input operably coupled to the first node of the bus, a second input operably coupled to a reference voltage, and an output coupled to the gate of the output transistor;

a mirror transistor having a gate operably coupled to the gate of the output transistor, a drain operably coupled to the gate of the output transistor, and a source;

a switch operably coupled between the source of the mirror transistor and the second node of the bus; and

a Miller capacitor coupled between the drain of the output transistor and the gate of the output transistor.

16. (Cancelled).

17. (Previously Presented) A method of providing a drive current to a bus, comprising: providing a first current to a gate of an output transistor during an inactive state, and providing a second current to the output transistor in an active state, and providing a third current to the output transistor when a voltage on the bus reaches a determined voltage,

Application Serial Number 10/535,656
Response to Office Action
Dated August 30, 2006

wherein the first current maintains a non-zero voltage at the gate of the output transistor.